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L4	2	2 or 3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/20 15:56
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Title - TTL (1):
Timer circuit and semiconductor memory incorporating the timer circuit

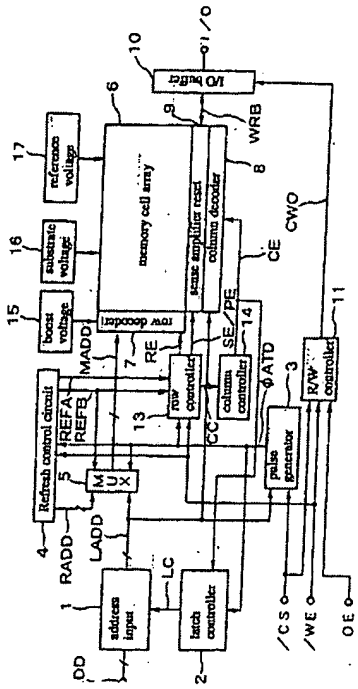
Summary of Invention Paragraph - BSTX (2):
[0001] The present invention relates to a timer circuit and a refresh control circuit having the timer circuit as well as a semiconductor memory device integrating the timer circuit, and more particularly to a word pulse generating circuit.

Summary of Invention Paragraph - BSTX (4):
[0002] DRAM is provided with memory cells, each of which comprises a data storage capacitor and a data transfer transistor. For storing data into the memory cell, a voltage corresponding to a logic value ("1" or "0") of the storage data is applied to the data storage capacitor to store a charge according to this voltage. In this data storage capacitor, a variety of current leak path is present, which causes that the charge accumulated in the data storage capacitor is gradually decreased over times, resulting in a deterioration of the data stored in the memory cell. For this reason, DRAM performs a cyclic or periodic refresh operation for refreshing the data of the memory cells.

Summary of Invention Paragraph - BSTX (5):
[0003] There is a variety of refresh methods, for example, a CAS before RAS for supplying, from outside, a necessary signal for refresh and an auto-refresh for refreshing in accordance with an address internally generated upon receiving an externally supplied trigger, and further a self-refresh for automatically refreshing inside. The semiconductor memory device utilizing the above-described self-refresh method integrates a timer circuit for generating a clock signal with a constant cycle, so that the lock signal generated by this timer circuit is counted to obtain a refresh timing without any external control.

Summary of Invention Paragraph - BSTX (9):
[0007] The current mirror circuit comprises three n-channel MOS transistors N1.about.N3 and two p-channel MOS transistors P1 and P2. The current mirror circuit controls a secondary current based on a primary current which flows through the above-described primary side load resistance RR. An input side of the ring oscillator is connected to a secondary side of the current mirror circuit, so that the ring oscillator acts as a load to the secondary side of the current mirror circuit. The ring oscillator comprises three inverters I1.about.I3 which are connected in ring-shape. Delay-purpose capacitors C1.about.C3 are respectively connected to output ports of the inverters I1.about.I3. An input port of the buffer circuit B is connected to an output port of the inverter I3, so that the buffer circuit B receives an input of an oscillation signal outputted from the inverter I3, and outputs a clock signal

FIG. 3



In this conventional technique, when the chip is in the standby state, most transistors are turned off, and only equalizers and some transistors operate, so that the leakage rate is relatively small. Under this condition, only the first Vbb generator Vbb-G1 which has a small driving capacity is driven, so that the power consumption can be reduced. Meanwhile, when the chip is active, or when the Vbb voltage level is below the predetermined level (-3 Vth), the second Vbb generator Vbb-G2 which has a large driving capacity is driven, so that the increase of the Vbb voltage due to the large current leakage through the driving of a large number of transistors can be prevented.

Brief Summary Text - BSTX (19):

The above described voltage generator for use in a conventional semiconductor memory device has a fixed oscillation period, and, therefore, it cannot accurately operate against the current leakage in a plurality of transistors in which the operation conditions are varied in the case of the active and standby conditions. That is, the oscillating frequency is decided by calculating the average of the current leakage. Further, the peak current for driving the large pumping capacitor becomes very high, thereby causing large voltage variations, as well as aggravating the reliability of the semiconductor memory device.

Brief Summary Text - BSTX (22):

Therefore, it is an object of the present invention to provide a voltage generator for use in a semiconductor memory device in which the oscillating period is controlled during the pumping operation to adjust the power generation pumped per unit of time, in such a manner that the voltage generator is suitable for use as a backbias voltage generator, as an internal high voltage generator, or as an internal power voltage generator, whereby the voltage is maintained at a constant level. Therefore, the charge pumping capacity is not adjusted by means of the pumping capacitor, but by the oscillation rate to adjust the pumping capacity to compensate for variations of the load. Accordingly, a large capacitor is not required, and the size of the transistor driving the pumping capacitor does not have to be large. Consequently, the peak current can be reduced, and the oscillating frequency (pulse rate) can be adjusted for the relevant purpose. Therefore, the charge pumping rate per unit of time can be increased or decreased in an easy manner.

Brief Summary Text - BSTX (23):

In achieving the above object, the voltage generator for use in a semiconductor device according to the present invention includes: a rectifier for producing a dc voltage power by rectifying clock signals; an oscillator including an odd number of invertors connected in series, and with the output of the last invertor fed back to the first invertor so as to oscillate clock pulses; and one or more bypass circuit connected so as for the output of the first invertor to bypass one or more intermediate invertors, and connected and disconnected by a control switch.

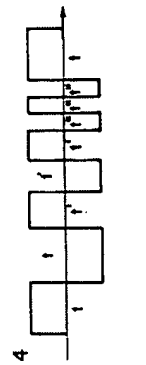


FIG. 4

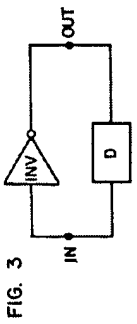


FIG. 3

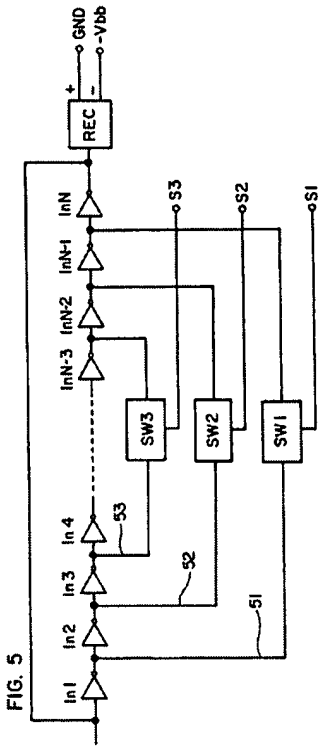


FIG. 5

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including an odd number of invertors connected in series, and with the output of the last invertor fed back to the first invertor so as to oscillate clock pulses; and one or more bypass circuit connected so as for the output of the first invertor to bypass one or more intermediate invertors, and connected and disconnected by a control switch.

Brief Summary Text - BSTX (28):
The first input terminals of the three 2-input NAND gate are connected to the oscillating circuit in series to receive the circulating signals, while their second input terminals receive a power stabilizing signal which is generated when the internal power voltage of the semiconductor memory device rises to a certain predetermined level.

Brief Summary Text - BSTX (29):
The control switch of the internal high voltage generator is turned on or off by the internal high voltage level detecting signals or by the word line enable signals.

Brief Summary Text - BSTX (30):
The bypass circuit forms: a first bypass circuit having a control switch which is turned on or off by the internal high voltage level detecting signals; and a second bypass circuit having a control switch which is turned on or off by the word line enable signals.

Drawing Description Text - DRTX (3):
FIG. 1 illustrates the circuit of the conventional voltage generator for use in a conventional semiconductor memory device;

Drawing Description Text - DRTX (4):
FIG. 2 is a block diagram showing the constitution of the internal backbias voltage generator for use in a conventional semiconductor memory device;

Detailed Description Text - DETX (3):
As shown in the block diagram of FIG. 5, invertors are serially arranged in the number of N (odd number), i.e., In1, In2, In3, In4, . . . Ini, . . . INN-3, INN-2, InN-1, InN. Further, rectifiers REC which are same as the conventional ones are connected to the output of the invertors, thereby generating dc power. Further, there are installed a plurality of bypass circuits 51, 52 and 53 for bypassing an arbitrary even number of the invertors. Bypassing is made by circulating oscillating signals Sg, so that the oscillating period can be controlled. Here, the plurality of the invertors perform the function of the inversion as shown in FIG. 3 and the function of delay. First, second and third control switches Sw1, Sw2 and Sw3 are inserted into the bypass circuits to connect or disconnect the bypass circuit. If the switch Sw1 is turned on to bypass the circulating oscillation signals through the first bypass circuit 51, the oscillation period becomes shortest (refer to

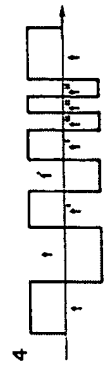

FIG. 4

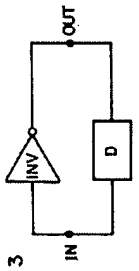

FIG. 3

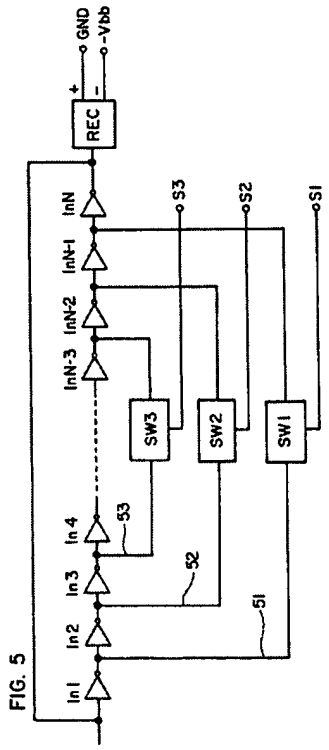

FIG. 5

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File Edit View Tools Window Help

EAST Advanced Search
Find what: 203
Find Next
Area: All, Sel/Cur
Direction: Up, Down
Match word: Whole, Part, Left, Right
Look in: Documents
Match case
Close
Help

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Abstract Text - ABTX (1):
A semiconductor device includes a word line drive circuit resetting the word line by driving the word line connected to a memory cell and switching a reset level of the word line drive circuit at the time of the reset operation of the word line. Further, a semiconductor device includes a memory cell array formed by arranging a plurality of memory cells and a reset level switch circuit for selecting a first potential or a second potential and supplying the first potential or the second potential to the word line drive circuit.

TITLE - TI (1):
Semiconductor memory device capable of driving non-selected word lines to first and second potentials

Brief Summary Text - BSTX (3):
The present invention relates to a semiconductor device having the function of executing a reset operation of a word line connected to a specific memory cell, by driving the word line in order to return the specific memory cell, in a memory cell array of a semiconductor memory, from an activated state to a standby state.

Brief Summary Text - BSTX (4):
Demands for lower power consumption have been increasing in recent years in semiconductor devices comprising a semiconductor memory such as a dynamic random access memory (hereinafter abbreviated to "DRAM") in consideration of battery driving. Therefore, power that is consumed in a circuit for executing the reset operation described above must be reduced as much as possible.

Brief Summary Text - BSTX (5):
The present invention also relates to a semiconductor device for shooting data by storing charges in memory cells and more specifically, to a semiconductor device which sets a word line potential at the time of non-selection to a negative potential so as to insure a safe and reliable operation even when a power source voltage is lowered so as to cope with higher circuit integration and even when a transistor threshold voltage value becomes low.

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Fig.5
PRIOR ART

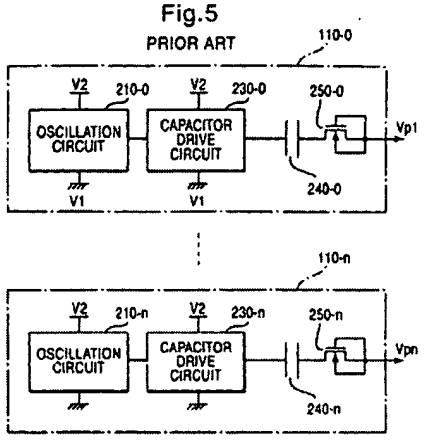
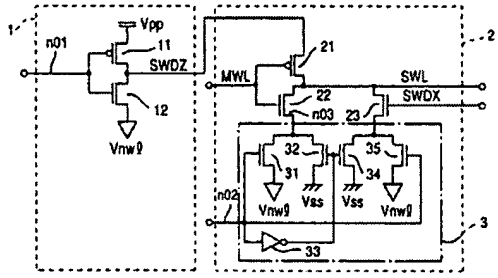


Fig.6



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